REMARKS

Claims 1-8 are pending in the present application. Claims 1 and 2 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

The drawings are objected to for reasons stated in the Office Action. The specification is amended above to properly include the reference character 19a. No new matter is added by the amendments to the specification. Entry of the amendment is respectfully requested.

The specification is objected to for reasons stated in the Office Action. The specification is amended above in a manner that is believed to be consistent with suggestions made in the Office Action. No new matter is added by the amendments to the specification. Entry of the amendments are respectfully requested.

Claim 1 stands objected to for an informality. Claim 1 is amended above in a manner that is believed to be consistent with suggestions made in the Office Action. Entry of the amendment is respectfully requested.

Claims 1, 2, 4, 6 and 8 stand rejected under 35 U.S.C. 102(a) as being anticipated by Divakaruni, *et al.* (U.S. Patent Number 6,727,539). Claims 1, 4 and 6 are rejected under 35 U.S.C. 102(a) as being anticipated by Takahashi (U.S. Patent Number 6,642,586). Claims 1, 3, 4, 5, 6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang, *et al.* (U.S. Patent Number 5,817,562 - hereinafter Chang '562). Claims 1, 2, 4, 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) in view of Chang, *et al.* (U.S. Patent Number 6,358,864 - hereinafter Chang '864). Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over each of Divakaruni, *et al.*, Takahashi, Chang '562 and Chang '864. Reconsideration of the rejections and allowance of claims 1-8 are respectfully requested.

Applicant notes that although the Office Action states at sections 7 and 8 that the rejections in view of Divakaruni, *et al.* and Takahashi are based on 35 U.S.C. 102(a), it is believed that 35 U.S.C. 102(e) is the intended and proper basis for these rejections.

In any event, it is respectfully submitted that Divakaruni, *et al.* and Takahashi are not applicable as prior art references against the present invention under 35 U.S.C. 102(a), under 35 U.S.C. 102(e) or under 35 U.S.C. 103(a)/102(a) or 35 U.S.C. 103(a)/102(e), since the present invention was invented before the United States filing date of both Divakaruni, *et al.* and Takahashi.

The present application was filed in the United States Patent and Trademark Office on November 12, 2003, as a divisional application under 35 U.S.C. 120 of United States Serial No. 09/994,154, filed November 26, 2001, which claims priority under 35 U.S.C. 119 to Korean application 01-6983, which was filed in the Korea Patent Office on February 13, 2001. Divakaruni, *et al.*, on the other hand, was filed in the United States Patent and Trademark Office on May 16, 2002 and is a divisional application of United States Serial No. 09/897,860, filed in the United States Patent and Trademark Office on July 2, 2001. Takahashi was filed in the United States Patent and Trademark Office on October 11, 2001.

The applicants submit herewith an English-language translation of the Korean application papers, KR01-6983 along with a statement by the translator that "...the statement in the English language in the attached translation of *Korean Patent Application No. 10-2001-0006983* consisting of *29* pages, have the same meanings as the statements in the Korean language in the original document, a copy of which I have examined.", which is believed to perfect the priority claim of the present United States application to the corresponding Korean application. With the benefit of the perfected claim of priority to the Korean application under 35 U.S.C. 119, the present application has an effective invention date of February 13, 2001. Since the invention date of February 13, 2001 of the present application is earlier than the U.S. filing date of Divakaruni, *et al.* (May 16, 2002) or the parent application of Divakaruni, *et al.* (July 2, 2001)

and since the invention date of February 13, 2001 of the present application is earlier than the U.S. filing date of Takahashi (October 11, 2001), it is submitted that Divakaruni, *et al.* and Takahashi are not applicable as prior art references under 35 U.S.C. 102(a) or 35 U.S.C. 102(e), with respect to claims 1, 2, 4, 6 and 8 and to claims 1, 4 and 6, respectively. It is further submitted that Divakaruni, *et al.* and Takahashi are not applicable as a prior art reference under 35 U.S.C. 103(a)/102(a) or 35 U.S.C. 103(a)/102(e), with respect to claim 7. Reconsideration and removal of the rejections based on Divakaruni, *et al.* and Takahashi are therefore respectfully requested.

In the present invention as claimed in independent claim 1, a semiconductor substrate having a multi-layered spacer, includes a plurality of gate electrodes each including a gate oxide layer, a gate conductive layer, and a capping dielectric layer formed on the semiconductor substrate. A gate polyoxide is layer formed on sidewalls of the gate oxide layer and the gate conductive layer and is in contact with a portion of the semiconductor substrate. A silicon nitride layer is in contact with sidewalls of the capping dielectric layer and in contact with the gate polyoxide layer. An oxide layer is in contact with an outer surface of the silicon nitride layer. An anisotropically etched external spacer is in contact with an outer surface of the oxide layer. A portion of the semiconductor substrate is exposed between neighboring gate electrodes by etching the oxide layer, silicon nitride layer and gate polyoxide layer using the external spacers and the gate electrodes as an etch mask so that outer ends of the gate polyoxide layer, the silicon nitride layer, and the oxide layer, and a lower outer end of the external spacer are aligned. A conductive pad is in a region between adjacent gate electrodes having the multi-layered spacer and is in contact with the exposed semiconductor substrate and the external spacer.

With regard to the rejection of claims 1, 3, 4, 5, 6, and 8 as being anticipated by Chang '562, it is submitted that Chang '562 fails to teach or suggest an "anisotropically etched external spacer" in contact with an outer surface of the oxide layer, as claimed in claim 1. The Office Action states that Chang '562 discloses at FIG. 5 "an oxide layer (28)" being in contact with silicon nitride layer 26 and "an external spacer (30)" in contact with the oxide layer. However,

the asserted Chang '562 "spacer" is described in the Chang '562 specification as a "conformal silicon nitride layer" (layer (30)) that is deposited on the underlying structure that includes sidewall spacers 7 (see Chang '52, column 6, lines 39-42). Thus, the Chang '562 layer 30 is not an "anisotropically etched external spacer" as claimed in claim 1.

In addition, Chang '562 fails to teach or suggest "a portion of the semiconductor substrate exposed between neighboring gate electrodes by etching the oxide layer, silicon nitride layer and gate polyoxide layer using the external spacers and the gate electrodes as an etch mask so that outer ends of the gate polyoxide layer, the silicon nitride layer, and the oxide layer, and a lower outer end of the external spacer are aligned", as claimed in amended claim 1. Layer 30 of Chang '562, asserted in the Office Action as being an "external spacer" is not used as an etch mask that results in alignment of "outer ends of the gate polyoxide layer, the silicon nitride layer, and the oxide layer, and a lower outer end of the external spacer", as claimed in amended claim 1. Instead, the Chang layer 30 is removed prior to etching the polysilicon oxide layer 24 (see Chang '562, FIG. 6), and the underlying spacer-shaped Chang '562 insulating layer 28 is used as a mask for etching the polysilicon oxide layer 24 (see Chang '562, FIG. 7). As a result, the Chang polysilicon oxide layer 24, and the silicon nitride layer 26 are aligned with the insulating layer 28, and not with the Chang '562 "external spacer" layer (30), since layer (30) was previously removed. It follows that Chang '562 fails to teach or suggest "a conductive pad ... in contact with the external spacer" as claimed in amended claim 1, since the asserted Chang '562 external spacer, i.e. layer (30), is removed prior to application of conductor layer (34) at FIG. 7 of Chang '562.

Accordingly, reconsideration of the rejection of independent claim 1 under 35 U.S.C. 102(e) as being anticipated by Chang '562, and allowance of the claim, are respectfully requested. With regard to the rejection of dependent claims 3, 4, 5, 6, 7 and 8 in view of Chang '562, it follows that these claims should inherit the allowability of independent claim 1, from which they depend.

With regard to the rejection of claims 1, 2, 4, 6, and 8 as being unpatentable over the combination of AAPA and Chang '864, it is submitted that Chang '864 fails to teach or suggest "a portion of the semiconductor substrate exposed between neighboring gate electrodes by etching the oxide layer, silicon nitride layer and gate polyoxide layer using the external spacers and the gate electrodes as an etch mask so that outer ends of the gate polyoxide layer, the silicon nitride layer, and the oxide layer, and a lower outer end of the external spacer are aligned" , as claimed in amended claim 1. Neither reference teaches or suggests this configuration that includes a silicon nitride layer disposed between the gate polyoxide layer and the external spacer.

With regard to Chang '864, oxide/nitride/oxide and oxide/nitride/oxide/nitride structures are well known structures for forming a multiple-layered dielectric films with reduced thickness and heightened insulative properties. In Chang '864, such a structure is used as a insulator between a floating gate and a control gate of a split-gate flash memory.

It is submitted that the AAPA and Chang '864 references are not properly combinable because they are from non-analogous arts. Though Chang '864 is in the field of semiconductor fabrication, the oxide/nitride/oxide/nitride structure of Chang '864 is for the purpose of forming a thin dielectric layer that is applied between a control gate and a floating gate of a split-gate flash memory structure. The AAPA oxide/oxide/nitride structure, on the other hand, is for the purpose of providing a protective region at a sidewall of a gate structure during various fabrication steps.

Even if combinable, the combined teachings of AAPA and Chang '864 do not teach or suggest the present invention as claimed in claim 1. In particular, neither reference teaches or suggests "a portion of the semiconductor substrate exposed between neighboring gate electrodes by etching the oxide layer, silicon nitride layer and gate polyoxide layer using the external spacers and the gate electrodes as an etch mask so that outer ends of the gate polyoxide layer, the silicon nitride layer, and the oxide layer, and a lower outer end of the external spacer are aligned", as claimed in claim 1. The combination does not teach or suggest such a structure, which, by virtue of the presence of the silicon nitride layer 110, the layer 110 can be used as an

etch stop layer during the self-aligned etching process, and further the silicon nitride layer 110 can serve as a blocking layer that bocks the penetration of carbon into the gate oxide layer 105 during later formation of pad 118.

In view of the above, it is submitted that neither AAPA, nor Chang '864, nor their combination, teach or suggest the invention as claimed in claim 1. Accordingly, reconsideration and removal of the rejection of, and allowance of, claim 1 is respectfully requested. With regard to the rejection of dependent claims 2, 4, 6, 7, and 8 in view of Chang '864 it is submitted these claims should inherit the allowability of independent claim 1.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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